19.8 A CMOS-Control Rectifier for Discontinuous-Conduction Mode Switching DC-DC Converters

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The power efficiency and inductor profile of switching dc-dc converters are two of the most important issues in modern battery-powered mobile systems. Discontinuous-conduction mode (DCM) operation enables both a reduction in the switching losses and the use of a small inductor, which are difficult to achieve in continuous-conduction mode (CCM) operation due to the high switching frequencies (10s to 100s of MHz) [1, 2]. However, adaptive dead-time control is necessary for high efficiency DCM switching dc-dc converters. In this paper, a CMOS-control rectifier (CCR) is proposed to simultaneously provide adaptive dead-time control and mV-range forward-voltage drop for sub-1V highly efficient DCM switching dc-dc converters employed in single-cell battery-powered mobile systems.

Figure 19.8.1 shows a DCM boost converter with the proposed CCR and the timing diagram. Adaptive dead-time control and mV-range forward-voltage drop are achieved in the CCR, which consists of a p-channel power transistor, comparators, and buffers. The proposed CCR conducts once the voltage V_X is equal to or larger than the output voltage V_{OUT}. Power loss caused by body-diode conduction and charge sharing between parasitic capacitor C_P and output capacitor C_{OUT} is minimized. Moreover, the CCR enables adaptive dead-time control that is insensitive to the variation of C_P with process. Since the proposed CCR behaves as a rectifier, conventional fixed dead-time control circuits and negative inductor-current sensing circuits can be eliminated. In addition, only one control signal (for switch S_1) is required, significantly simplifying the design of the controller.

A block diagram and complete schematic of the proposed CCR are shown in Fig. 19.8.2. A p-channel power transistor M_P with large aspect ratio (W/L) is employed to provide mV-range forward-voltage drop. The body terminal of M_P is connected to the output terminal of the CCR to prevent any unwanted reverse current through the intrinsic body diode of M_P. The conduction state of transistor M_P is determined by sensing the voltage difference across it using two cross-coupled comparators, A_1 and A_2. The coupling-capacitor C_C simultaneously provides transient latching-action and stable dc operation. As shown in Fig. 19.8.2, the source node of transistors M_{11}, M_{12}, M_{21} and M_{22} is employed as the input of the comparators, which solves the common-mode voltage limitation in differential-input comparators with current-tail bias. Moreover, transistors M_{b1} and M_{b2} are used to provide a dc bias-voltage for transistor M_{23}. To ensure that transistor M_P can be fully turned off, all three inverting buffers are supplied from the output of the proposed CCR.

A boost converter with the proposed CCR and control circuitry is shown in Fig. 19.8.3. Since the boost converter is designed for single-cell (e.g., nickel-based battery) battery-powered mobile systems, the control circuitry should be able to operate at 0.9V, the minimum voltage of a nickel-based battery. To avoid the use of a complex comparator with rail-to-rail input common-mode range, the pulse width modulation (PWM) signal is produced by comparing a fixed dc voltage V_{DC} to a ramp, which is generated by the voltage-to-current converter, the timing capacitor C_t and the reset transistor M_{SET}. As a result, the design of the control circuitry is significantly simplified. Moreover, the output voltage of the boost converter is used as the supply voltage of the buffer circuit for the n-channel power transistor M_N, minimizing the on-resistance of power transistor M_N, and, hence, improving power efficiency.

Both the proposed CCR and the boost converter with CCR have been implemented in Austria Micro Systems (AMS) 0.35µm 2-poly 4-metal CMOS technology. Fig. 19.8.4 shows the on and off characteristics of the proposed CCR with a 1µH inductor. The use of cross-coupled comparators in the proposed CCR facilitates nanosecond response times, which is proven by the measured on-time T_{ON} (~20ns) and the measured off-time T_{OFF} (~60ns). As shown in Fig. 19.8.4, the proposed CCR provides mV-range forward-voltage drop and the conduction loss is significantly lower than silicon or Schottky diodes. Therefore, the efficiency of boost converters, especially those with sub-1V input, can be improved simply by replacing the diodes with CCRs.

The boost converter with the CCR provides a regulated output voltage of 2.5V with 100mA maximum output current. The input voltage range is from 0.9 to 1.2V. Switching loss is minimized by operating the boost converter at 667kHz. Moreover, a 4.7µF output capacitor and a 1µH inductor are used to facilitate the application of the entire boost converter to modern pocket-size, or even thumb-size, mobile systems. Fig. 19.8.5 shows the output voltage V_{OUT}, the switching node voltage V_X and the inductor current I_L of the boost converter with the CCR. When V_{IN} is 1.2V, the converter operates in DCM. Once V_{IN} drops to 0.9V, the converter operates very near to the DCM/CCM boundary when I_{OUT} equals 100mA. As shown in Fig. 19.8.5, the switching-node voltage V_X rings when the inductor current I_L is zero. This ringing is characteristic of DCM operation, and can easily be suppressed with a freewheel switch [3]. The measured power efficiency is shown in Fig. 19.8.6. Maximum power efficiency of ~ 87% is achieved at 100mA output current and 1.2V input voltage. Even when the input voltage drops to 0.9V, ~ 85% efficiency is obtained at 100mA output current. The chip area of the boost converter is 3mm^2, and the chip micrograph is shown in Fig. 19.8.7.

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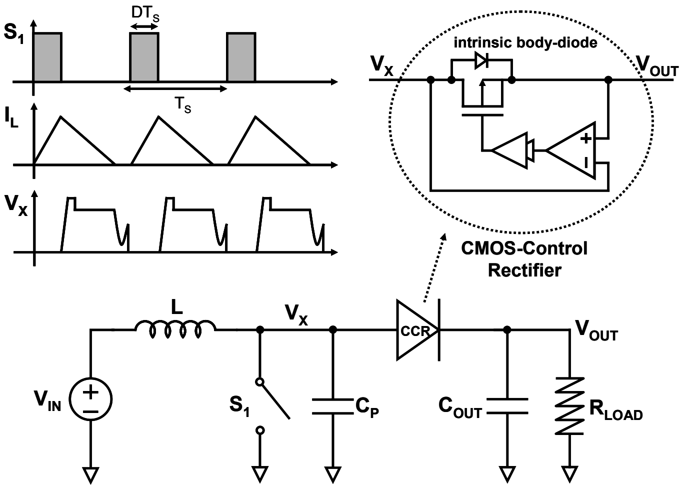

Figure 19.8.1: Simplified schematic and timing diagram of a DCM boost converter with CCR.

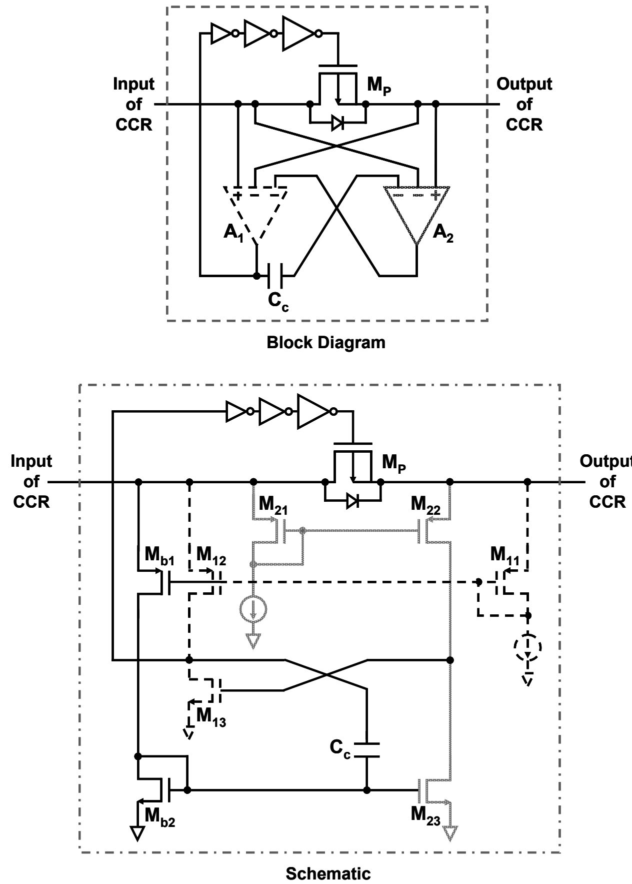

Figure 19.8.2: Block diagram and schematic of CCR.

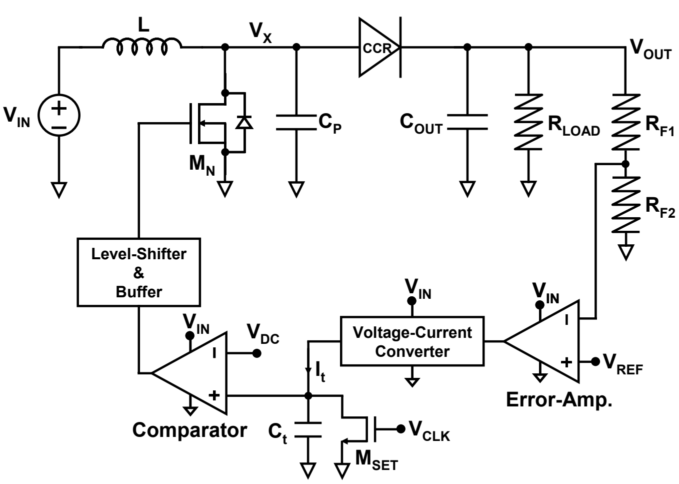

Figure 19.8.3: Control circuitry of a DCM boost converter with a CCR.

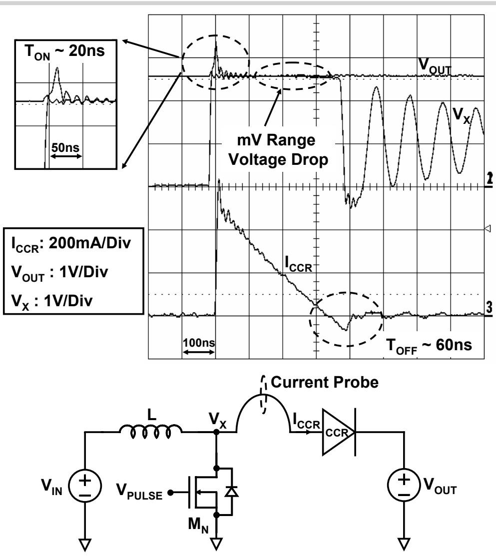

Figure 19.8.4: On and off characteristics of a CCR.

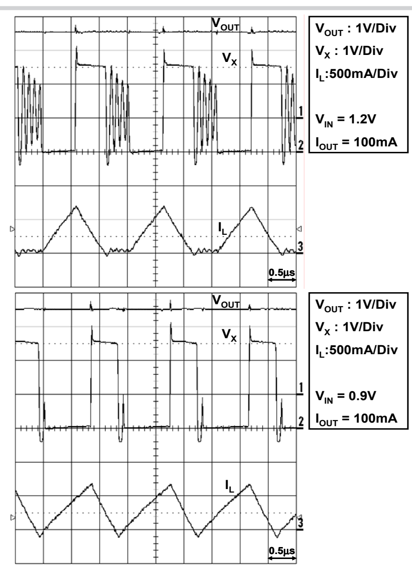

Figure 19.8.5: Measurement results of a DCM boost converter with CCR.

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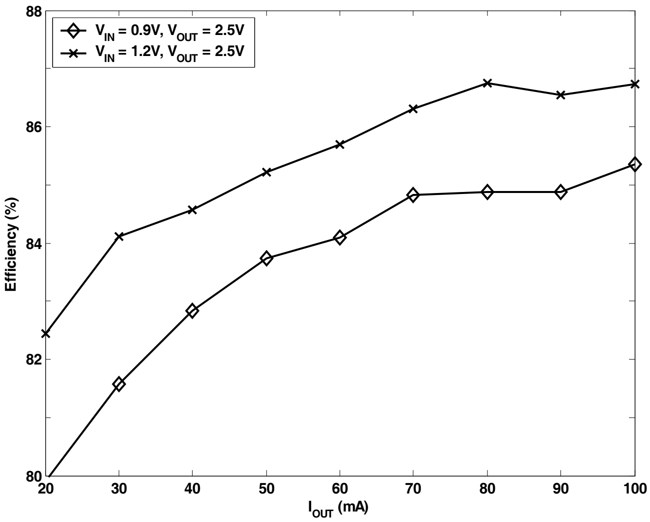

Figure 19.8.6: Power efficiency of a DCM boost converter with CCR.

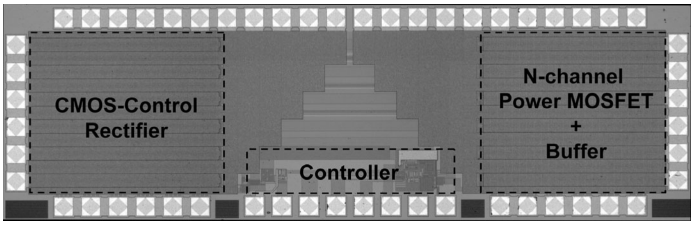

Figure 19.8.7: Chip micrograph of a DCM boost converter with CCR.